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EXAMINER

ABEL JALIL, NEVEEN

ART UNIT	PAPER NUMBER
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2175

15

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/923,262

Applicant(s)

NAGARAJA, SRIKANTH

Examiner

Neveen Abel-Jalil

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-60 is/are pending in the application.
- 4a) Of the above claim(s) 31-44 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15-30 and 45-60 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- 1) ☐ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


SAM RIMELL
PRIMARY EXAMINER

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

1. The Request for Reconsideration filed on March 17, 2004 has been received and entered. Claims 1-60 are pending in the application. Of the above claims, 1-15, and 31-44 are withdrawn from consideration.

2. The Specification has been amended. Therefore, the rejection under 112 1st paragraph is hereby withdrawn.

3. Corrections to claims 15, 16, 45, and 46 have been made.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 15-30, and 45-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melli et al. (U.S. Pub. No. 2002/0111699 A1) in view of Dyer et al. (U.S. Patent No. 6,625,592 B1) as best taught and understood.

As to claim 15, Melli et al. discloses a method of performing a search function in an integrated circuit (See page 3, paragraph 0030), the method comprising the steps of:

storing a table in a table memory in the integrated circuit (See page 3, paragraphs 0030-0034);

inputting a search key (See page 2, paragraphs 0024-0026);

performing at least one search function on the table in the operational plane memory using the search key (See page 3, paragraph 0032, also see page 2, paragraph 0024).

Melli et al. does not teach transferring substantially simultaneously the table in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function.

Dyer et al. teaches transferring substantially simultaneously the table in parallel from the table memory to an operational plane memory in the integrated circuit (See column 5, lines 4-45); and outputting a result of the at least one search function (See column 5, lines 35-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Melli et al. to include transferring substantially simultaneously the table in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Melli et al. by the teaching of Dyer et al. to include transferring substantially simultaneously the table in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function because it allows for faster processing and more efficient use of the integrated circuitry in a computer.

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As to claim 16, Melli et al. discloses a method of performing a search function in an integrated circuit (See page 3, paragraph 0030), the method comprising the steps of:

storing a plurality of tables in a table memory in the integrated circuit (See page 3, paragraphs 0030-0034);

inputting a table identifier, the table identifier being representative of one of the plurality of sorted tables (See page 3, paragraph 0030, and also see pages 3-4, paragraph 0035);

inputting a search key (See page 2, paragraphs 0024-0026);

performing at least one search function on the at least one table in the operational plane memory using the search key (See page 3, paragraph 0032, also see page 2, paragraph 0024).

Melli et al. does not teach transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and

outputting a result of the at least one search function.

Dyer et al. teaches transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit (See column 5, lines 4-45); and

outputting a result of the at least one search function (See column 5, lines 35-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Melli et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function.

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It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Melli et al. by the teaching of Dyer et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function because it allows for faster processing and more efficient use of the integrated circuitry in a computer.

As to claim 17, Melli et al. as modified discloses comprising the step of coupling the integrated circuit to at least one of a microprocessor (See Dyer et al. column 3, lines 57-678, and see Dyer et al. column 4, lines 1-5), a microcontroller, and an application specific integrated circuit (ASIC) (See Melli et al. page 3, paragraph 0030).

As to claim 18, Melli et al. as modified discloses comprising the step of arranging at least one of the table memory and the operational plane memory as a multi-dimensional array of memory (See Dyer et al. column 5, lines 47-64, also see Melli et al. page 3, paragraphs 0028-0030).

As to claim 19, Melli et al. as modified discloses comprising the step of arranging at least one of the table memory and the operational plane memory in at least one column, at least one row, and at least one table (See pages 3-4, paragraphs 0035-0036).

As to claim 20, Melli et al. as modified discloses comprising the steps of:

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arranging the at least one column as an array of bytes (See Dyer et al. column 4, lines 22-61);

arranging the at least one row as an array of columns (See Dyer et al. column 3, lines 8-56); and

arranging the at least one table as an array of rows (See Dyer et al. figure 3).

As to claim 21, Melli et al. as modified discloses comprising the step of storing the result in at least one register in the integrated circuit, the at least one register being accessible to at least one device external to the integrated circuit (See Dyer et al. column 3, lines 32-44, also see Dyer et al. column 5, lines 1-34).

As to claim 22, Melli et al. as modified discloses comprising the steps of:

inputting a command to at least one register in the integrated circuit (See Dyer et al. column 3, lines 57-67, and see Dyer et al. column 4, lines 1-41);

interpreting the command by the integrated circuit (See page 2, paragraphs 0014-0019);
and

initiating an action in the integrated circuit in response to the command (See page 4, paragraphs 0035-0036, wherein “response to command” reads on “process the request”).

As to claim 23, Melli et al. as modified discloses wherein the command is representative of one of specifying a portion of the storage circuit in which to store at least one of the plurality of tables (See page 1, paragraph 0002), initiating storage of the plurality of tables in the storage

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circuit, specifying the at least one table stored in the storage circuit on which to perform the at least one search function (See page 3, paragraphs 0029-0030), specifying at least one search key, specifying the at least one search function, and initiating the at least one search function (See page 3, paragraphs 0032-0034).

As to claim 24, Melli et al. as modified discloses comprising the step of inputting a search function identifier, the search function identifier being representative of one of the plurality of search functions, the integrated circuit, performing the at least one search function represented by the search function identifier (See page 3, paragraphs 0029-0032, also see Dyer et al. column 3, lines 32-67).

As to claim 25, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the step of performing the at least one search function being performed in parallel on the plurality of entries of the at least one table (See Dyer et al. column 5, lines 1-34).

As to claim 26, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the result including at least one of the plurality of entries that equals a search key (See Dyer et al. column 5, lines 65-67, and see Dyer et al. column 6, lines 1-16).

As to claim 27, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the result including at least two of the plurality of entries between which a

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search key is located (See page 2, paragraphs 0020-0021).

As to claim 28, Melli et al. as modified discloses wherein the at least one search function performed includes at least one of a sequential and a parallel N-ary search (See page 3, paragraphs 0030-0031).

As to claim 29, Melli et al. as modified discloses wherein the step of transferring one of the plurality of tables substantially simultaneously in parallel (See Dyer et al. column 5, lines 1-34) from the table memory to the operational plane memory in the integrated circuit is performed in response to the integrated circuit receiving an initiate search command (See page 2, paragraphs 0014-0020, also see page 2, paragraphs 0026, and see page 3, paragraph 0030).

As to claim 30, Melli et al. as modified discloses comprising the step of modifying the at least one table while the at least one table is in the operational plane memory (See page 2, paragraph 0022, also see Dyer et al. column 7, lines 34-65).

As to claim 45, Melli et al. discloses a method of performing a search function, the method comprising the steps of:

inputting unsorted entries (See page 2, paragraphs 0020-0021, wherein “unsorted” reads on “generic”);

performing a hash function on the unsorted entries, the hash function arranging the unsorted entries into a sorted table (See pages 3-4, paragraph 0035);

storing the sorted table in a table memory in an integrated circuit (See page 3, paragraphs 0030-0034);

inputting a search key (See page 2, paragraphs 0024-0026);

performing at least one search function on the sorted table in the operational plane memory using the search key (See page 3, paragraph 0032, also see page 2, paragraph 0024).

Melli et al. does not teach transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and

outputting a result of the at least one search function.

Dyer et al. teaches transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit (See column 5, lines 4-45); and

outputting a result of the at least one search function (See column 5, lines 35-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Melli et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Melli et al. by the teaching of Dyer et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the

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integrated circuit; and outputting a result of the at least one search function because it allows for faster processing and more efficient use of the integrated circuitry in a computer.

As to claim 46, Melli et al. discloses a method of performing a search function, the method comprising the steps of:

inputting unsorted entries (See page 2, paragraphs 0020-0021, wherein “unsorted” reads on “generic”);

performing a first hash function on the unsorted entries, the first hash function arranging the unsorted entries into a plurality of sorted tables (See pages 3-4, paragraph 0035);

storing the plurality of sorted tables in a table memory in an integrated circuit (See page 3, paragraphs 0030-0034);

inputting a search key (See page 2, paragraphs 0024-0026);

performing a second hash function on the search key, the second hash function outputting a table identifier (See page 3, paragraph 0032, also see page 2, paragraph 0024),

the table identifier being representative of one of the plurality of sorted tables in which the search key is likely to be found (See page 3, paragraphs 0029-0030, also see figure 5, 262);

performing at least one search function on the at least one table in the operational plane memory using the search key (See page 2, paragraphs 0024-0025).

Melli et al. does not teach transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and

outputting a result of the at least one search function.

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Dyer et al. teaches transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit (See column 5, lines 4-45); and

outputting a result of the at least one search function (See column 5, lines 35-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Melli et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Melli et al. by the teaching of Dyer et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function because it allows for faster processing and more efficient use of the integrated circuitry in a computer.

As to claim 47, Melli et al. as modified discloses wherein the steps of performing a first hash function and performing a second hash function are performed by at least one of a microprocessor (See Dyer et al. column 4, lines 1-5), a microcontroller, and an application specific integrated circuit (ASIC) (See Melli et al. page 3, paragraph 0030).

As to claim 48, Melli et al. as modified discloses comprising the step of arranging at least one of the table memory and the operational plane memory as a multi-dimensional array of memory (See Dyer et al. column 7, lines 21-33, also see Dyer et al. column 8, claim 1 language).

As to claim 49, Melli et al. as modified discloses comprising the step of arranging at least one of the table memory and the operational plane memory in at least one column, at least one row, and at least one table (See pages 3-4, paragraphs 0035-0036).

As to claim 50, Melli et al. as modified discloses comprising the steps of:
arranging the at least one column as an array of bytes (See Dyer et al. column 4, lines 22-61);
arranging the at least one row as an array of columns (See Dyer et al. column 3, lines 8-56); and
arranging the at least one table as an array of rows (See Dyer et al. figure 3).

As to claim 51, Melli et al. as modified discloses comprising the step of storing the result in at least one register in the integrated circuit, the at least one register being accessible to at least one device external to the integrated circuit (See Dyer et al. column 5, lines 1-34).

As to claim 52, Melli et al. as modified discloses comprising the steps of:
inputting a command to at least one register in the integrated circuit (See Dyer et al. column 3, lines 57-67, and see Dyer et al. column 4, lines 1-41);

interpreting the command by the integrated circuit (See page 2, paragraphs 0014-0019);
and

initiating an action in the integrated circuit in response to the command (See page 4, paragraphs 0035-0036, wherein “response to command” reads on “process the request”).

As to claim 53, Melli et al. as modified discloses wherein the command is representative of one of specifying a portion of the storage circuit in which to store at least one of the plurality of tables (See page 1, paragraph 0002), initiating storage of the plurality of tables in the storage circuit, specifying the at least one table stored in the storage circuit on which to perform the at least one search function (See page 3, paragraphs 0029-0030), specifying at least one search key, specifying the at least one search function, and initiating the at least one search function (See page 3, paragraphs 0032-0034).

As to claim 54, Melli et al. as modified discloses the method further comprising the step of inputting a search function identifier, the search function identifier being representative of one of the plurality of search functions, the integrated circuit performing the at least one search function represented by the search function identifier (See page 3, paragraphs 0029-0032, also see Dyer et al. column 3, lines 32-67).

As to claim 55, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the step of performing the at least one search function being performed in

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parallel on the plurality of entries of the at least one table (See Dyer et al. column 5, lines 1-34).

As to claim 56, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the result including at least one of the plurality of entries that equals a search key (See Dyer et al. column 5, lines 65-67, and see Dyer et al. column 6, lines 1-16).

As to claim 57, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the result including at least two of the plurality of entries between which a search key is located (See page 2, paragraphs 0020-0021).

As to claim 58, Melli et al. as modified discloses wherein the at least one search function performed includes at least one of a sequential and a parallel N-ary search (See Dyer et al. column 7, lines 21-33, also see Dyer et al. column 8, claim 1 language).

As to claim 59, Melli et al. as modified discloses wherein the step of transferring one of the plurality of tables substantially simultaneously in parallel (See Dyer et al. column 5, lines 1-34) from the table memory to the operational plane memory in the integrated circuit is performed in response to the integrated circuit receiving an initiate search command (See page 2, paragraphs 0014-0020, also see page 2, paragraphs 0026, and see page 3, paragraph 0030).

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As to claim 60, Melli et al. as modified discloses comprising the step of modifying the at least one table while the at least one table is in the operational plane memory (See page 2, paragraph 0022, also see Dyer et al. column 7, lines 34-65).

Response to Arguments

6. Applicant's arguments filed on March 17, 2004 have been fully considered but they are not persuasive.

In response to applicant's argument that "Melli et al. does not teach the substantially simultaneous transfer of the table from operational plane memory to table memory, as now defined by the amended claims 15, 16, 45, and 46" is respectfully acknowledged but is not deemed to be persuasive.

The Examiner respectfully points to Melli et al. pages 3-4, paragraphs 0033-0039, also see page 2-3, paragraphs 0025-0027, wherein the data structure of the invention is stored in a memory and referenced by pointers. The data structure can be stored and read from in any form of memory as disclosed by Melli et al. on page 4, paragraph 0039; after it was created by the generic object factory in the table memory at run time as taught on page 2, paragraph 0014. And it can be searched as indicated by page 2, paragraph 0022, wherein "search" reads on "look-up".

However, Melli et al. is combined with reference Dyer et al. to teach this feature as suggested by the office action and therefore they are treated in combination and not separately therefore please see response to argument below.

In response to applicant's argument that "Dyer et al. does not teach or suggest transferring substantially simultaneously at least one complete table to be searched in parallel from table memory to operational plane memory and then performing a search function on that table in a separate portion of memory, that is operational plane memory, as now defined by the amended claims 15, 16, 45, and 46" is respectfully acknowledged but is not deemed to be persuasive.

The Examiner respectfully points to Dryer et al. column 7, lines 4-38, wherein the transferring a copy (updated or original) of the hash table stored in the memory to different linked computers and linked memories is taught; and wherein, the hash table that permits the user to have search requests is implemented in shared memory is also taught. All the above operations are being done in "a single step" as disclosed in Dryer et al. column 5, lines 4-45, and wherein the search is stored in records in a table located in shared memory also see column 4, lines 21-41.

However, Melli et al. is combined with reference Dyer et al. to teach this feature as suggested by the office action and therefore they are treated in combination and not separately therefore please see response to argument above.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

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USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner is establishing motivation in obviousness in the knowledge generally available to one of ordinary skill in the art, to modify the invention of Melli et al. with the teachings of Dryer et al., as explained in the above office action. The Examiner refers the applicant to Dryer et al. column 2, lines 7-49 to find the motivation to combine presented by the Examiner. Dryer et al. teaches a more efficient search method that is faster and less CPU-intensive.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neveen Abel-Jalil whose telephone number is 703-305-8114.

The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on 703-305-3830. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Neveen Abel-Jalil
May 30, 2004


SAM RIMELL
PRIMARY EXAMINER